Method and Structure of Manufacturing High Capacitance Metal On Insulator Capacitors in Copper

ABSTRACT OF THE DISCLOSURE

An improved semiconductor integrated circuit device structure. The device structure includes a substrate. A thickness of first insulating material is overlying the substrate. A capacitor region within the thickness of the first insulating material and extends from a lower surface of the first insulating material to an upper surface of the first insulating material. The capacitor region includes a width, which extends from the lower surface to the upper surface. The width may vary slightly in some embodiments. The structure includes a contact region overlying the substrate within at least the capacitor region. A lower capacitor plate formed from a plurality of vertical metal structures defined within the capacitor region and connected to the contact region. Each of the plurality of vertical metal structures includes a width and a height. Each of the plurality of vertical metal structures is substantially parallel to each other along a length of the height of each of the vertical metal structures. A barrier metal layer is formed overlying exposed surfaces of each of the plurality of vertical metal structures. A capacitor dielectric layer is overlying each of the exposed surfaces of the barrier layer on each of the vertical metal structures. An upper capacitor plate is formed from metal material within the capacitor region overlying surfaces of the capacitor dielectric layer. The device structure also has a planarized surface formed from the upper capacitor plate in preferred embodiments.